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floorplanning,
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... taking the
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as an input and
generating edge
and ...

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the legendary
555 has found
favor both with
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the IC are still
being ...

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the effort to
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without a
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to create a core-independent function that ordinarily would have to be created with an external IC. One of the biggest benefits to this configuration
...

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... "These requirements ...

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fabrication is
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model,
extraction tools
use the design's
physical layout

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to identify the
nets most likely
to have a bridge
between them.

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servers, and ...

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novel IC design

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program that
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**eFabless Joins
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multi-headed
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with up to four
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of the security
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for generating
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sizes can
dominate the
global micro
server IC
market. The
reduced size of
chips can
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workflow For a
three-phase
electric motor
to be
controlled, we

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have to provide
proper voltage
to the motor by
reading phase
current I_a , I_b ,
 I_c . Without
having a ...
SVM's role is to
...

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control
algorithm
enhances motor**

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Global
application
specific IC
market was
valued at US\$
16,250.0 Mn
market in 2018
and is
forecasted to
reach a value of
US\$ 61,348.0 Mn
by 2027 at a

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CAGR of 7.4%
between 2017 and
2027.

Analog IC Market
Advanced
Technology
Analysis,
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employs a
strategic
methodological
approach that
considerably
aids businesses
in generating
revenues and

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Expansion by

2027 | Fujitsu

Semiconductor,

Renesas

Electronics

Due to the

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ionizing nature
of space
radiation, that
radiation can
often affect
devices by
generating a
charge inside
silicon-based
... radiation
immunity due to
their device
physics and
layout. The ...

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In this
partnership,
open source
designs were
selected to be
fabricated at no
cost to
designers. The

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submission
process was open
for 30 days,
generating 1700
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and generating
sales exceeding
€250 million
across three
established
brands. Grupo
Halcón will
reinvigorate the
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new catalogue of

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**Grupo Halcón, a
leading ceramic
tile
producer,...**

The project, to
be matched with
\$400,000 in
local funds, is
expected to
create 21 jobs

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and generate \$1
million in
private
investment. The
grants are aimed
"to diversify
the regional
economy and ...

**Osage Nation
drone program,
Fab Lab Tulsa
awarded \$2.5
million in**

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federal grants
and generating
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across three
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This book
presents an
innovative
methodology for
the automatic
generation of
analog
integrated
circuits (ICs)
layout, based on

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template
descriptions and
on evolutionary
computational
techniques. A
design
automation tool,
LAYGEN II was
implemented to
validate the
proposed
approach giving
special emphasis
to reusability

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of expert design
knowledge and to
efficiency on
retargeting
operations.

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In this book,
innovative
research using
artificial
neural networks
(ANNs) is
conducted to
automate the

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placement task
in analog
integrated
circuit layout
design, by
creating a
generalized
model that can
generate valid
layouts at push-
button speed.
Further, it
exploits ANNs'
generalization

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and push-button
speed prediction
(once fully
trained)
capabilities,
and details the
optimal
description of
the input/output
data relation.
The description
developed here
is chiefly
reflected in two

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of the system's
characteristics:
the shape of the
input data and
the minimized
loss function.
In order to
address the
latter, abstract
and segmented
descriptions of
both the input
data and the
objective

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behavior are
developed, which
allow the model
to identify, in
newer scenarios,
sub-blocks which
can be found in
the input data.
This approach
yields device-
level
descriptions of
the input
topology that,

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for Layouts With
focus on
describing its
relation to
every other
device in the
topology. By
means of these
descriptions, an
unfamiliar
overall topology
can be broken
down into
devices that are

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subject to the
same constraints
as a device in
one of the
training
topologies. In
the experimental
results chapter,
the trained ANNs
are used to
produce a
variety of valid
placement
solutions even

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beyond the scope
of the training/
validation sets,
demonstrating

the model's
effectiveness in
terms of
identifying

common
components
between newer
topologies and
reutilizing the
acquired

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Lastly, the methodology used can readily adapt to the given problem's context (high label production cost), resulting in an efficient, inexpensive and fast model.

Integrated

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Generating Og
circuits are With
fundamental
electronic
components in
biomedical,
automotive and
many other
technical
systems. A
small, yet
crucial part of
a chip consists
of analog
circuitry. This

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part is still in
large part
designed by hand
and therefore
represents not
only a
bottleneck in
the design flow,
but also a
permanent source
of design errors
responsible for
re-designs,
costly in terms

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of wasted test
chips and in
terms of lost
time-to-market.

Layout design is
the step of the
analog design
flow with the
least support by
commercially
available,
computer-aided
design tools.

This book

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provides a
survey of
promising new
approaches to
automated,
analog layout
design, which
have been
described
recently and are
rapidly being
adopted in
industry.

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This title

covers important
physical-design
issues that

exist in

contemporary
analogue and
mixed-signal

design flows.

The authors
bring together
many principles
and techniques
required to

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successfully
develop and
implement layout
generation tools
to accommodate
many mixed-
signal layout
generation
needs.

This book
applies to the
scientific area
of electronic

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design Layouts With
automation (EDA)
and addresses
the automatic
sizing of analog
integrated
circuits (ICs).
Particularly,
this book
presents an
approach to
enhance a state-
of-the-art
layout-aware

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circuit-level
optimizer (GENOM-
POF), by
embedding
statistical
knowledge from
an automatically
generated
gradient model
into the multi-
objective multi-
constraint
optimization
kernel based on

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the NSGA-II With
algorithm. The
results showed
allow the
designer to
explore the
different trade-
offs of the
solution space,
both through the
achieved device
sizes, or the
respective
layout

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This book
introduces
readers to a
variety of tools
for automatic
analog

integrated
circuit (IC)
sizing and
optimization.

The authors
provide a

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historical
perspective on
the early
methods proposed
to tackle
automatic analog
circuit sizing,
with emphasis on
the
methodologies to
size and
optimize the
circuit, and on
the

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methodologies With
estimate the
circuit's
performance. The
discussion also
includes robust
circuit design
and optimization
and the most
recent advances
in layout-aware
analog sizing
approaches. The
authors describe

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a methodology
for an automatic
flow for analog
IC design,
including
details of the
inputs and
interfaces,
multi-objective
optimization
techniques, and
the enhancements
made in the base
implementation

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by using machine learning techniques. The Gradient model is discussed in detail, along with the methods to include layout effects in the circuit sizing. The concepts and algorithms of all the modules

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are thoroughly
described,
enabling readers
to reproduce the
methodologies,
improve the
quality of their
designs, or use
them as starting
point for a new
tool. An
extensive set of
application
examples is

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is included to
demonstrate the
capabilities and
features of the
methodologies
described.

This book
introduces
readers to a
variety of tools
for analog
layout design
automation.

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After discussing
the placement
and routing
problem in
electronic
design
automation
(EDA), the
authors overview
a variety of
automatic layout
generation
tools, as well
as the most

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recent advances
in analog layout-
aware circuit
sizing. The

discussion

includes
different
methods for

automatic

placement (a

template-based

Placer and an op

timization-based

Placer), a fully-

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automatic Router
and an empirical-
based Parasitic
Extractor. The
concepts and
algorithms of
all the modules
are thoroughly
described,
enabling readers
to reproduce the
methodologies,
improve the
quality of their

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designs, or use
them as starting
point for a new
tool. All the
methods
described are
applied to
practical
examples for a
130nm design
process, as well
as placement and
routing
benchmark sets.

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Analog

integrated
circuits are
very important
as interfaces
between the
digital parts of
integrated
electronic
systems and the
outside world. A

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large portion of
the effort
involved in
designing these
circuits is
spent in the
layout phase.

Whereas the
physical design
of digital
circuits is
automated to a
large extent,
the layout of

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is still a
manual, time-
consuming and
error-prone
task. This is
mainly due to
the continuous
nature of analog
signals, which
causes analog
circuit
performance to
be very

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sensitive to
layout
parasitics. The
parasitic
elements
associated with
interconnect
wires cause
loading and
coupling effects
that degrade the
frequency
behaviour and
the noise

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performance of
analog circuits.
Device mismatch
and thermal
effects put a
fundamental
limit on the
achievable
accuracy of
circuits. For
successful
automation of
analog layout,
advanced place

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and route tools
that can handle
these critical
parasitics are
required. In the
past, automatic
analog layout
tools tried to
optimize the
layout without
quantifying the
performance
degradation
introduced by

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Therefore, it was not guaranteed that the resulting layout met the specifications and one or more layout iterations could be needed. In Analog Layout Generation for

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Performance and
Manufacturabilit
y, the authors
propose a
performance
driven layout
strategy to
overcome this
problem. In this
methodology, the
layout tools are
driven by
performance
constraints,

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Is Layouts With
such that the
final layout,
with parasitic
effects, still
satisfies the
specifications
of the circuit.
The performance
degradation
associated with
an intermediate
layout solution
is evaluated at
runtime using

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predetermined With
sensitivities.
In contrast with
other
performance
driven layout
methodologies,
the tools
proposed in this
book operate
directly on the
performance
constraints,
without an

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intermediate With
parasitic
constraint
generation step.

This approach
makes a complete
and sensible
trade-off
between the
different layout
alternatives
possible at
runtime and
therefore

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eliminates the
possible
feedback route
between
constraint
derivation,
placement and
layout
extraction.
Besides its
influence on the
performance,
layout also has
a profound

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layouts the
yield and
testability of
an analog
circuit. In
Analog Layout
Generation for
Performance and
Manufacturabilit
y, the authors
outline a new
criterion to
quantify the
detectability of

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le Layouts With
combine this
with a yield
model to
evaluate the
testability of
an integrated
circuit layout.

They then
integrate this
technique with
their
performance
driven routing

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algorithm to
produce layouts
that have
optimal manufact
urability while
still meeting
their
performance
specifications.
Analog Layout
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y will be of

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interest to With
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engineers,
researchers and
students.

Sciences And
This book covers
the fundamental
knowledge of
layout design
from the ground
up, addressing
both physical
design, as

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applied to
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circuits, and
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Such knowledge
provides the
critical
awareness and
insights a
layout designer
must possess to
convert a
structural

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description With
produced during
circuit design
into the
physical layout
used for IC/PCB
fabrication. The
book introduces
the
technological
know-how to
transform
silicon into
functional

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devices, to
understand the
technology for
which a layout
is targeted
(Chap. 2). Using
this core
technology
knowledge as the
foundation,
subsequent
chapters delve
deeper into
specific

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constraints and
aspects of
physical design,
such as
interfaces,
design rules and
libraries (Chap.
3), design flows
and models
(Chap. 4),
design steps
(Chap. 5),
analog design
specifics (Chap.

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6), and finally
reliability
measures (Chap.
7). Besides
serving as a
textbook for
engineering
students, this
book is a
foundational
reference for
today's circuit
designers.

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